ABSTRACT

A chemical mechanical polishing (CMP) step is used to remove excess conductive material (e.g., Cu) overlying a low-k or ultralow-k interlevel dielectric layer (ILD) layer having trenches filled with conductive material, for a damascene interconnect structure. A reactive ion etch (RIE) or a Gas Cluster Ion Beam (GCIB) process is used to remove a portion of a liner which is atop a hard mask. A wet etch step is used to remove an oxide portion of the hard mask overlying the ILD, followed by a final touch-up Cu CMP (CMP) step which chops the protruding Cu patterns off and lands on the SiCOH hard mask. In this manner, processes used to remove excess conductive material substantially do not affect the portion of the hard mask overlying the interlevel dielectric layer.